## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system comprising:

a memory;

a logic system coupled to the memory; and

a processor coupled to the memory wherein the processor comprises;

an execution pipeline; and

a digital throttle coupled to the execution pipeline, wherein the digital throttle is to estimate a power state, responsive to activity of the execution pipeline, and to trigger one of a plurality of power-control mechanisms, responsive to the estimated power state reaching a first threshold.

2. (Original) The system of claim 1, wherein the power control mechanisms include adjusting instruction throughput of the execution pipeline and adjusting an operating point for the execution pipeline.

3. (Original) The system of claim 1, wherein the digital throttle comprises an activity monitor to provide an activity level responsive to activity states of units of the execution pipeline, a conversion unit to estimate the power state from the activity level, and a threshold unit to trigger a first power control mechanism, responsive to the power state reaching the first threshold.

4. (Original) The system of claim 3, wherein the digital throttle triggers a second power control mechanism responsive to an indication that the second power control mechanism is warranted.

5. (Original) The system of claim 3, wherein the digital throttle includes a mode unit to monitor an output of the threshold unit and to trigger the second power control mechanism, responsive to the output reaching a second threshold.

6. (Currently Amended) The system of claim 5, wherein the first power control mechanism ~~is~~ adjusts instruction throughput for the execution pipeline and the second power control mechanism adjusts an operating point to the execution pipeline

7. (Original) The system of claim 1, further comprising a mode unit to switch from a first power control mode to second power control mode, responsive to the first power control mode reaching a saturation condition.

8. (Currently Amended) A method comprising:

monitoring an activity level of a processor to determine a power state;

~~triggering one of a plurality of power control mechanisms;~~

activating a first power control mechanism if the power state meets a first threshold;

monitoring a status associated with the first power control mechanism; and

activating a second power control mechanism responsive to the monitored status.

9. (Original) The method of claim 8, wherein the status is a counter that indicates a level of power control provided by the first power control mechanism and activating the second power control mechanism comprises activating the second power control mechanism, responsive to the counter reaching a threshold value.

10. (Original) The method of claim 9, wherein the counter tracks a number of times the first power control mechanism is activated or a duration for which the first power control mechanism is activated.

11. (Original) The method of claim 8, wherein activating the first power control mechanism comprises adjusting instruction throughput for the processor, responsive to the power state reaching the first threshold.

12. (Original) The method of claim 11, wherein activating the second power control mechanism comprises adjusting an operating point of the processor, responsive to the monitored status.

13. (Currently Amended) An apparatus comprising:

an execution pipeline including one or more units to execute instructions;

an activity monitor to estimate an activity level for the processor, responsive to a activity states of the one or more units;

a throttle circuit to trigger a first power mode ~~to estimate a power state, to trigger one of a plurality of power control mechanisms~~, responsive to a power state determined from the estimated activity level reaching a first threshold; and

a mode ~~circuit~~ unit to track a status associated with the first power mode and to trigger a second power mode, responsive to the status reaching a second threshold.

14. (Original) The apparatus of claim 13, wherein the status is a counter value that tracks usage of the first power mode and the mode circuit triggers the second power mode if the usage reaches the second threshold.

15. (Original) The apparatus of claim 14, wherein the counter tracks a number of times the first power mode is triggered or an interval for which the first power mode is active.

16. (Original) The apparatus of claim 13, wherein the first power mode adjusts instruction throughput for the execution pipeline and the second power mode adjusts an operating point for the execution pipeline.

17. (Original) The apparatus of claim 16, wherein the second power mode specifies one of multiple combinations of voltage and frequency values at which the execution pipeline may be operated.

18. (Original) The apparatus of claim 17, wherein the mode unit initiates the second power mode at a first of the combinations and selects a new combination, responsive to an estimated power state for the execution pipeline operating under the first combination.

19. (Original) The apparatus of claim 17, wherein the mode unit deactivates the second power mode responsive to the power state for the execution pipeline operating under a current combination reaching a fourth threshold.